Highly Linear RF CMOS Amplifier and Mixer Adopting MOSFET Transconductance Linearization by Multiple Gated Transistors

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Abstract — **A highly linear CMOS RF amplifier and mixer circuits adopting MOSFET transconductance linearization by linearly superposing several common-source FET transistors in parallel, combined with some additional circuit techniques such as cascode for amplifier and harmonic tuning for mixer, are reported. Experimental result designed using above techniques shows IP3 improvements at given power consumption by as large as 10 dB for RF amplifier at 900 MHz and 7 dB for Gilbert cell mixer at 2.4 GHz without sacrificing other features such as gain and NF.**

I. Introduction

Linearity in RF system is quite an important issue because nonlinearity brings many problems such as, gain compression, cross modulation and intermodulation, etc. the 3rd order intermodulation distortion (IMD3) is the most dominant nonlinearity component and thus most popularly used parameter for measurement. The performance measure for this nonlinearity is usually expressed by IP3 (the 3rd order intercept point)/DC power consumption.

Among many other fabrication technologies, CMOS is believed to the most promising technology as system on a chip solution, especially for low cost and low power system such as Bluetooth and WLAN operating at ISM band which is very crowded with various applications which could be played as interferers, thus, it is utmost important for CMOS to have IP_3/DC as large as possible to be competitive.

Several circuit techniques have been proposed to improve linearity of RF amplifier. Because most of them are based on negative feedback circuits, the enhancement in linearity is the result of the gain reduction which is the characteristics of negative feedback. Actually, circuit linearity is ultimately limited by MOSFET transistor linearity, which is the Common Source (CS) MOSFET transconductance. In the area of mixer circuits, Gilbert cell is certainly one of the best candidates suitable for monolithic integration. It is composed of RF transconductance amplifier and switching stage, and its linearity is mostly determined by that of transconductance.

Therefore it is very important to linearize MOSFET transconductance for both RF amplifier and mixer circuits. We have shown that multiple gated transistor (MGTR) [1] is an effective way to linearize CS MOSFET neither using extra power consumption nor adding any process change. However, it is also shown that the obtained IP3/DC improvement is much smaller than that expected from linearity improvement in transconductance. In this work, we propose that the use of MGTR combined with other circuit techniques can indeed improve IP3/DC by an order of magnitude. We show the design and fabrication results for 900 MHz CMOS amplifier with IP3/DC improvement as large as 10 dB which is obtained by adopting MGTR combined with cascode configuration, as for the mixer, we obtained 7dB IP3/DC improvement at 2.4 GHz adopting MGTR and 2nd harmonic termination techniques without sacrificing other RF characteristics such as gain and NF.

II. Cascode MGTR CMOS Amplifier

Non-linearity of CS FET amplifier mostly comes from transconductance (g_m) nonlinearity in the driving MOSFET transistor. Using Taylor series expansion, the drain current of a CS FET can be expressed as (1).

$$i_{DS} = I_* + g_m v_{gs} + \frac{g_m'}{2!} v_{gs}^2 + \frac{g_m''}{3!} v_{gs}^3 + \dots \quad (1)$$

Here v_{gs} is a small signal gate-to-source voltage and $g_m^{(n)}$ indicates n_{th} derivative of effective trasconductance with respect to v_{gs}.

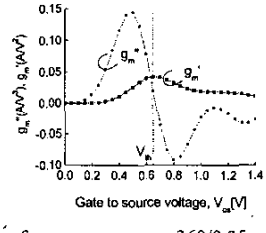

Fig. 1 g_m'' and g_m' of a common source 360/0.35 μm MOSFET.

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It is well known that the coefficient of v_{gs}^3 in (1) plays an important role in determining the IMD3 of an RF amplifier [1]. As we can see in Fig. 1 that g_m'' has negative peak value in the gate drive voltage range of 0.1~ 0.45 V (gate-to-source voltage range of 0.76 V~1.11 V in Fig. 1), which is the usual bias voltage for high gain, low noise and low power applications [1]. Thus linearity degradation is quite severe. In MGTR amplifier, however, this negative peak of MT(main transistor) can be cancelled by the positive peak value of properly sized ST (secondary transistor) whose transfer characteristics is shifted to the right by changing either the gate bias or the threshold voltage as shown in Fig. 2. Note that, because ST is biased in subthreshold regime, this linearization method does not require any extra power consumption.

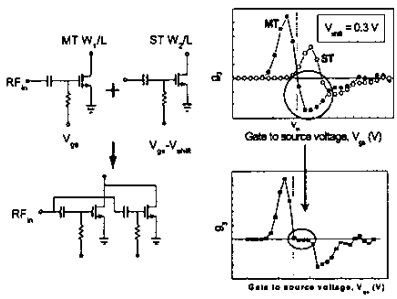

Fig. 2 Schematic illustration of g_m'' cancellation using MGTR. The size and gate bias of ST is chosen such that the negative g_m'' peak of MT is cancelled by the positive one of ST.

As was introduced before, although MGTR can effectively reduce g_m'' almost to zero, we cannot obtain IP3/DC not more than 3-5 dB. In [2], we show that the 3rd order distortion caused by the combination of g_m' and harmonic feedback becomes dominant in highly linearized tranconductance amplifier having very small g_m''. It may be possible to reduce these effects using out-of-band termination.

The effect of out-of-band termination on intermodulation distortion was originally analyzed for bipolar common emitter amplifier circuit [3], which can be applied to FET one as follows,

$$IIP3 = \frac{1}{6\,\mathrm{Re}\{Z_S(\omega)\}\cdot|H(\omega)|\cdot|A_1(\omega)|^3\,|\varepsilon(\Delta\omega,2\omega)|} \quad (2)$$

$$\varepsilon(\Delta\omega,2\omega) = g_m'' - g_{OB} \quad (3)$$

where,

$$g_{OB} = \frac{2(g_m')^2}{3}\left[\frac{2}{g_m + g(\Delta\omega)} + \frac{1}{g_m + g(2\omega)}\right] \quad (4)$$

Here Z_s indicates the source impedance and $g(\Delta\omega)$ and $g(2\omega)$ are the conductance functions to be defined at sub-harmonic frequency, $\Delta\omega$ and, 2nd harmonic frequency, 2ω, respectively. $H(\omega)$ is related to equivalent IMD3 voltage to the IMD3 response of the drain current nonlinear term and $A_1(\omega)$ is linear transfer fuction for the input voltage of v_{gs} [2], [3]. $\varepsilon(\Delta\omega, 2\omega)$ shows the relationship how drain current works for IMD3 response. In (3) g_m'' comes from 3rd order nonlinearity in drain current and g_{OB} comes from the combined effect of 2nd order nonlinearity generating 2nd order product which is then mixed with the fundamental tones yielding 3rd order products [3]. This self-interaction is due to multiple feedbacks in the circuit mainly by gate-drain capacitance [3]. Eq. (2)-(4) implies that, linearity (IP3) improvement can indeed be improved firstly by reducing g_m'', but that, as can be seen in (3), when g_m'' becomes negligibly small, $\varepsilon(\Delta\omega, 2\omega)$ becomes dominated by g_{OB} which is proportional to square of g_m' (see (4)). As can be inferred from Fig. 1, although g_m'' peak can effectively be cancelled using MGTR, the value of g_m' is still appreciable. Therefore we have to devise some way to decrease g_{OB}. One of the best way to achieve this is to increase both $g(\Delta\omega)$ and $g(2\omega)$.

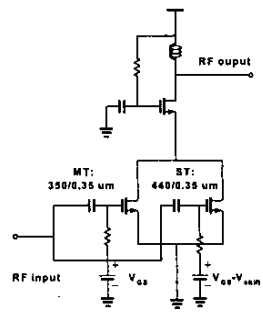

Fig. 3 Simplified schematic of Cascode MGTR amplifier.

In CS FET circuit as shown in Fig. 3, $g(2\omega)$ was originally defined in [3], which can be approximately given as,

$$g(2\omega) \approx g_m \times \frac{1 + 2j\omega C_{gs} Z_1 + 2j\omega C_{gd} Z_2}{1 + \omega_T C_{gd} Z_2}. \quad (5)$$

Here Z_1 and Z_2 are the impedance looking into the source and that into the load respectively and ω_T is the unit current cutoff angular frequency defined as $\omega_T = g_m/C_{gs}$. Note that $g(\Delta\omega)$ is much larger compared with $g(2\omega)$.

In typical CS FET amplifier, the magnitude of Z_1 is of the order of $1/(\omega C_{gs})$. Thus the second term in the numerator of (5) is comparable to 1. Furthermore, because $2\omega << \omega_T$,

$\omega_T C_{gd} Z_2$ in the denominator is the most dominating factor. Therefore it is very important to reduce $\omega_T C_{gd} Z_2$ smaller than 1. In other words, Z_2 should be decreased as much as possible. In [3] harmonic tuning is used to reduce Z_2. In this work, however, we propose to use cascode configuration to reduce Z_2 for LNA. In cascode configuration, Z_2 is decreased to $1/g_m$. Although this is not as good as the harmonic tuning, our approach is more plausible because it provides as good performance as the harmonic tuning method and does not require large passive L, C components as in [3].

III. HARMONIC TUNED MGTR MIXER

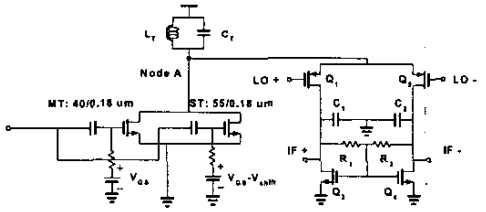

Fig. 4 Simplified schematic of harmonic tuned MGTR mixer.

Now let us show highly linear mixer using MGTR in the transconductance combined with harmonic tuning, which was adopted for the amplifier circuits. Fig. 4 shows circuit schematic diagram for this circuits, which is composed of LC-folded cascode mixer and MGTR transconductor. L_T and C_T are resonant at ω, providing maximum load for the signal, while short at 2nd harmonic frequency of 2ω as well as at sub-harmonic frequency of $\Delta\omega$. As was discussed for amplifier case, it is well known that $\Delta\omega$, 2ω components at common source node (node A in Fig. 4) worsen the linearity in conventional single balanced mixer, which is greatly reduced using peaking circuit in Fig. 4. Moreover, linearization using MGTR is most effective when the driver FET used for transconductance amplifier is in saturation region, i.e., at large V_{ds}. The folded cascode circuit in Fig. 4 helps us to have large voltage headroom for V_{ds}, making the driver FET always in saturation region.

IV. DESIGN AND FABRICATION OF CASCODE MGTR AMPLIFIER AND HARMONIC TUNED MIXER

A. 900 MHz Cascode MGTR amplifier

900 MHz cascode MGTR amplifier whose schematic is shown in Fig. 3 is designed and fabricated using only CMOS in 0.35 μm SiGe BiCMOS process. The MT is typically biased at gate drive ($V_{GT}=V_{gs}-V_{th}$, where V_{th}=0.66 V) of 0.24 V and V_{GT} of ST is negative, i.e., ST is in subthreshold regime when there is no input signal. Fig. 5 shows the measured IMD3 reduction vs. V_{GT} of ST, while V_{GT} of MT is fixed at 0.24 V. Note that maximum IMD3 reduction as large as 20dB is obtained. Fig. 6 shows the measured IP3 at maximum IMD3 reduction and comparison of conventional cascode amplifier. Note that IP3 improvement at least as large as 10 dB is obtained from proposed cascode MGTR over the 0.13 V window of V_{GT} variation of ST, which is wide enough to cover process variation. The OIP3 of the proposed amplifier is 25.6 dBm at 7.8 mA current consumption. Measurement performance comparison with conventional one are summarized in Table. 1. Although it has slightly higher NF (note NF is simulated one) because of ST, it improves IP3 order of magnitude.

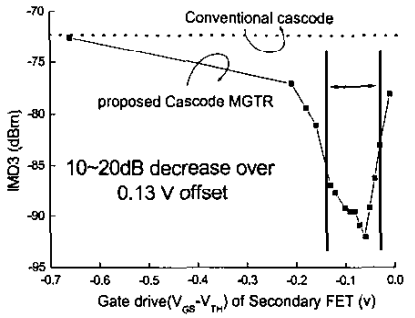

Fig. 5 IMD3 reduction vs ST gate drive voltage of cascode MGTR amplifier.

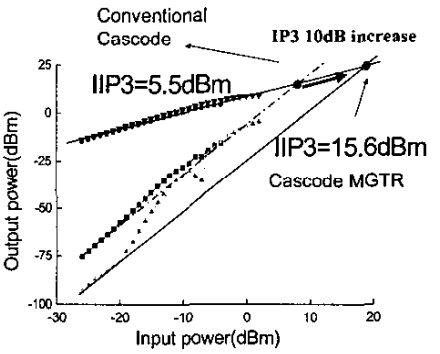

Fig. 6 IP3 comparison between conventional cascode and cascode MGTR amplifier.

B. Harmonic Tuned MGTR Mixer

2.4 GHz harmonic tuned MGTR mixer with LC folded cascode structure shown in Fig. 4 is designed and fabricated using 0.18 μm CMOS technology. MT is biased at gate drive of 0.14 V(V_{th}=0.48 V) and ST bias is below V_{th} Fig. 7 shows measured IP3 increase vs. V_{GT} of ST where MT is fixed at V_{GT} of 0.14 V. Maximum IP3 increase is 7 dB and IP3 improvement is 5~7 dB over 0.1 V range which can cover process variation. Fig. 8 shows the measured IP3 at maximum IMD3 reduction and comparison of conventional LC folded cascode mixer which have only one transistor at transconductor stage. Measurement result summarized in Table. 2. The result show us IP3 increase is almost order of magnitude while gain and NF degradation because of ST is insignificant.

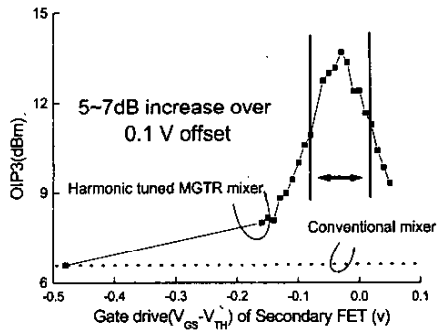

Fig. 7 IP3 increase vs. ST gate drive voltage for harmonic tuned MGTR mixer.

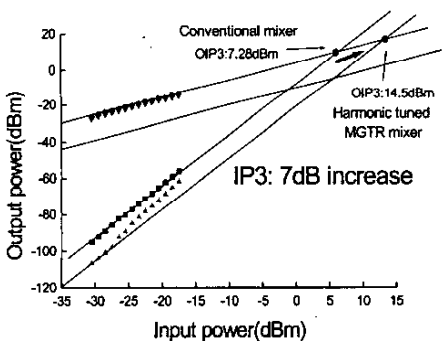

Fig. 8 IP3 comparison between conventional mixer and harmonic tuned MGTR mixer.

Table. 1 Measurement summary of cascode MGTR amplifier.

	Conventional cascode	Cascode MGTR
Power Gain	10 dB	10 dB
IIP3	5.5 dBm	15.6 dBm
NF	2.25 dB	2.85 dB
Current , Vdd=2.7V	7.45mA	7.82 mA

Table. 2 Measurement summary of conventional mixer and harmonic tuned MGTR mixer.

	Conventional cascode	Harmonic tuned MGTR
Voltage Gain(4MHz IF)	16 dB	16.5 dB
IIP3	2.5 dBm	9 dBm
DSB NF	13.3 dB	14.2 dB
Current , Vdd=1.8V	2.9mA	3 mA

V. Conclusion

A highly linear CMOS RF amplifier and mixer circuits adopting MOSFET transconductance linearization by linearly superposing several common-source FET transistor in parallel (multiple gated transistor, MGTR), combined with some additional circuit techniques such as cascode for amplifier and harmonic tuning for mixer, are reported. Experimental results designed using above techniques show IP3 improvements at given power consumption by as large as 10 dB for RF amplifier at 900 MHz and 7 dB for Gilbert cell mixer at 2.4 GHz without sacrificing other features such as, gain and NF.

Acknowledgement

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